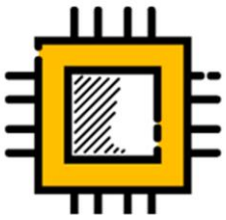
VERIFICATION OF VIDEO SOC



CHIPMONK

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BACKGROUND

The Client had developed a proprietary IP block that converted raw video frames into GigE-Vision packets, enabling transmission over an ethernet network to multiple devices.

There was interest by customers to use this IP as a part of a larger SoC system that coordinated communication between a host processor and multiple capture devices over an ethernet network. The client had developed an SoC reference design and required Chipmonk's verification expertise to achieve silicon success.

DELIVERABLES

EDA VENDOR MANAGEMENT

The SoC contained industry-standard interfaces and required the purchase of off-the-shelf VIP. The DFT architecture also required BIST and SCAN insertion tools. The evaluation of different vendor options was a key part of the initial groundwork done by Chipmonk's engineers.

VERIFICATION OF SOC REFERENCE DESIGN – 95% COVERAGE GOAL

The verification goal was 95% functional coverage + 95% statement/branch/toggle coverage. The coverage numbers were focused on the IP and specific SoC blocks that were developed by the Client. External IPs are verified by the vendor and coverage would only focus on the specific functionality that is required for the Client use-case.

CONSTRAINED-RANDOM TEST SUITE + TESTBENCH FOR IP

The development of a standalone randomized testbench for the Client IP that could be delivered to customers was one of the key requirements of the project. When integrating the IP, customers should have the ability to run a suite of functional tests to ensure the correct operation. This reduces engineering cost and debug cycles.

FIRMWARE VALIDATION ON FPGA PLATFORM

The Client IP was being emulated on a Xilinx Virtex-7 FPGA. The requirement was to convert UVM sequences into low-level C code that could be run on the FPGA platform for enhancing testing capabilities (4K frames consume too much simulation time).

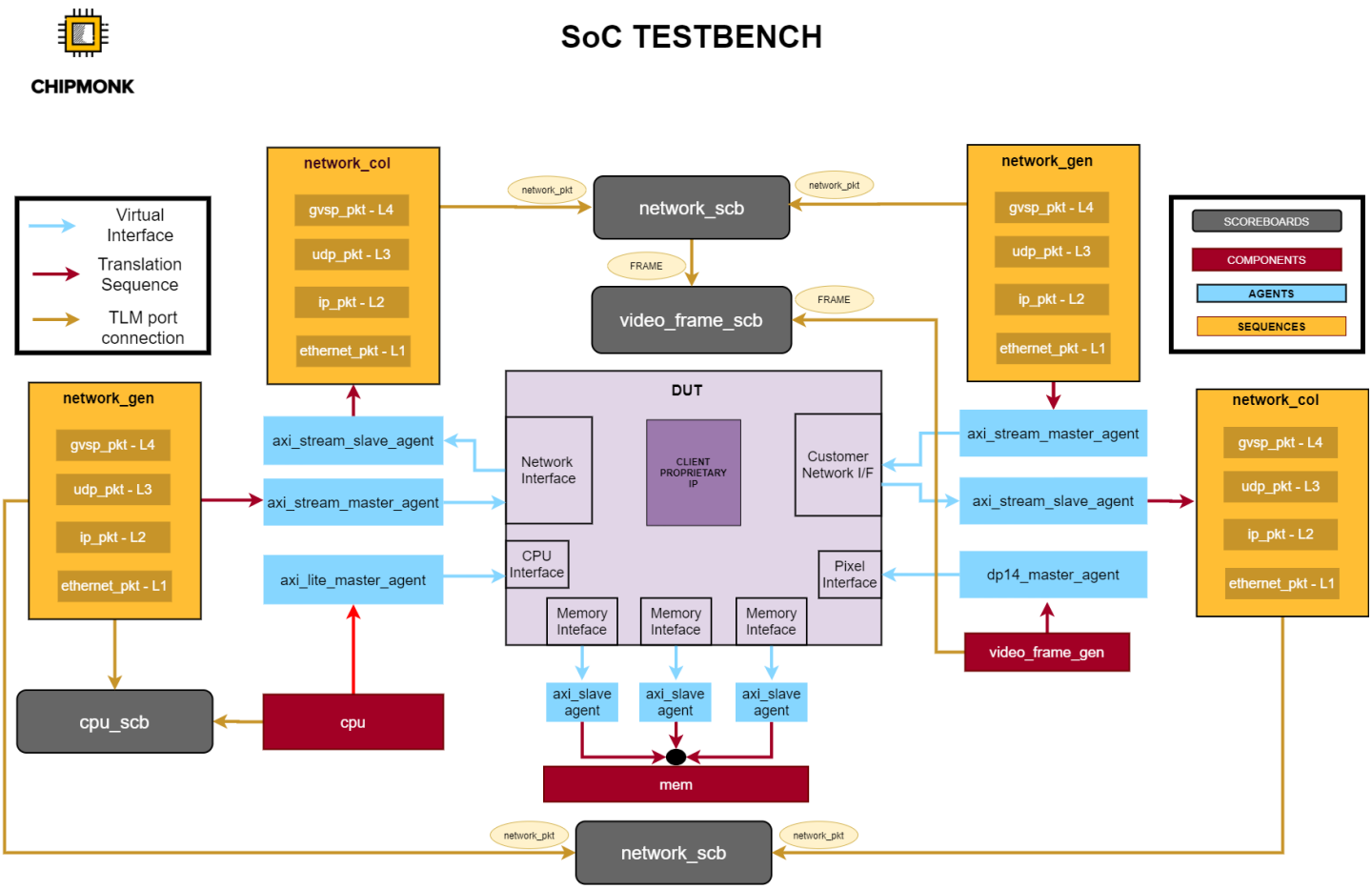
TIMELINE

MONTH 0-1 PLANNING PHASE (L1)	MONTH 2-4 BRINGUP PHASE (L2)	MONTH 5-10 RTL FREEZE PHASE (L3)	MONTH 10-12 TAPEOUT PHASE (L4)
Architecture Spec (Design Team) Testplan writing and review Ramp-up team on technology, IP design, protocols EDA Vendor evaluation and decision Architecture and Design Document review Testbench Architecture finalized	Interface Freeze (Design Team) Interface assertions written and connected. Functional coverage writing (covergroups, coverpoints) VIP integration and custom agent development (scoreboards, agents and checkers) Test sequence development – sanity directed testcases Code Coverage goal – 25%	RTL Freeze (Design Team) Random test sequence development Compliance testing DFT Insertion and testing (MBIST and Scan insertion) Translation of programming sequences into C-code (Firmware) Regression debug (80% passing) Code Coverage goal – 80%	PD Signoff (Design Team) ECO window – close critical path items Post PnR gate-level sims IP test suite completed (coding and documentation) Firmware tests running on FPGA prototype Feature and Performance tests Regression debug (99%) Code Coverage goal (99% w/ waivers reviewed) Verification Spec completed

TECHNOLOGY STACK

Ethernet 802.3 | GigE Vision | DisplayPort 1.4 | I2C SMBUS | AMBA AXI3

TESTBENCH ARCHITECTURE



RESULT

The Client taped out the SoC reference design as an MPW test chip in 16nm FF+ technology after a 12-month verification window and had customers sampling silicon after 16 months.

The engagement was a success with all major feature sets being fully functional. Performance targets were met as well. The combination of working silicon & verified IP and test-suite allowed the Client to secure multiple design wins.